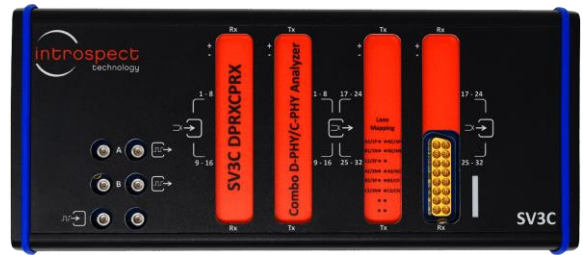


# SV3C-DPRXCPRX

## Combo MIPI D-PHY/C-PHY Analyzer



### All-in-One Protocol Analyzer for Camera and Display Interface Links

The SV3C-DPRXCPRX Combo MIPI D-PHY/C-PHY Analyzer is an ultra-portable, high-performance instrument for testing and validating MIPI-based transmitters as well as probing live systems. The SV3C-DPRXCPRX is ideal for the capture and analysis of MIPI transmitters used in cameras, displays, and other devices. It includes integrated LP and HS receivers, dynamic termination, and a range of sophisticated features including bus turn-around (BTA) and compression picture parameter set (PPS) handling. The SV3C-DPRXCPRX is ideal for both MIPI physical layer transmitter port testing and full protocol layer testing.

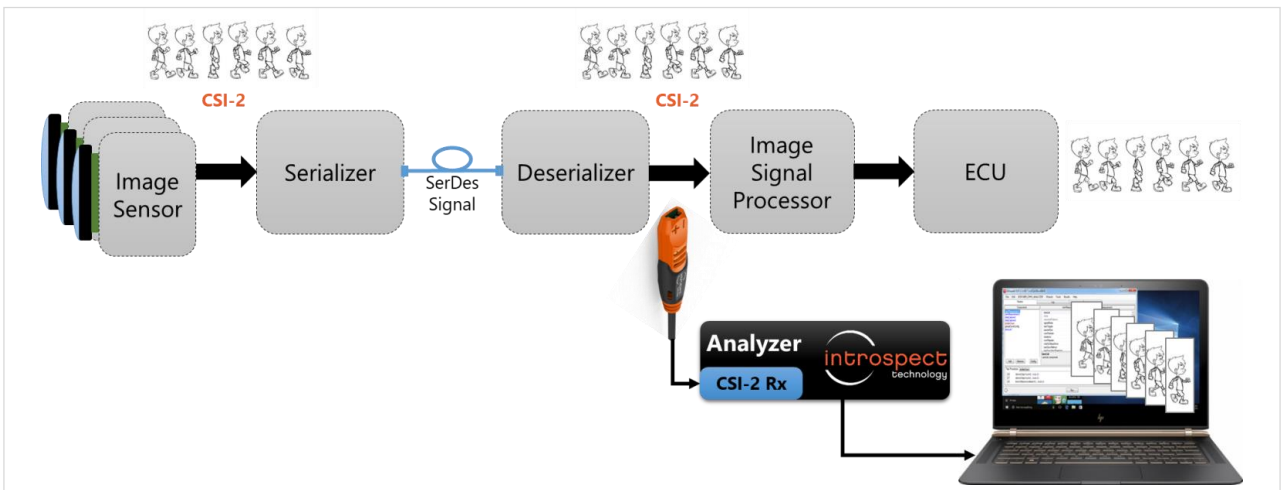
#### KEY FEATURES:

- **Wide data rate support:** fully continuous range from 80 Mbps to 4.5 Gbps (D-PHY) / 3.5 Gbps (C-PHY)
- **High resolution timing analysis:** physical layer and protocol layer events are recorded and analyzed for conformance
- **Waveform measurement and analysis:** verify signal integrity within a live in-system environment
- **Hardware CRC and image checking:** unlimited counting durations

#### KEY BENEFITS:

- **Future proof:** wide data rate coverage ensures that the same instrument can cover many product variants and design generations
- **Self-contained:** an all-in-one system reduces bench space and helps create a portable test and measurement environment; the SV3C integrates multiple tools into one
- **Automated:** scripting capability is ideal for debug tasks, physical-layer and protocol-layer conformance testing, and full-fledged production screening of devices and system modules.

### Typical Application: Automotive Camera System Test and Debug



## Transmitter Parameters

Receiver Parameter	Description		Benefit
	D-PHY	C-PHY	
<b>Number of Differential Receivers</b>	4 Data + 1 Clock	4 Trios	Flexible configuration and coverage for multi-lane applications
<b>HS Differential Detectable / Allowable Voltage Swing</b>	90 – 600 mV	90 – 500 mV	Coverage for D-PHY and C-PHY Transmitter CTS specifications
<b>LP Differential Programmable Threshold Voltage Swing</b>	-100 – 1500 mV	-100 – 1500 mV	Coverage for D-PHY and C-PHY Transmitter CTS specifications
<b>Total Memory Space</b>	4 GByte	4 GByte	Deep vector memory allows for tracing and debugging long-term events

## Environment and Control

Feature	Description	Benefit
<b>DUT Control Interface</b>	I2C master, software programmable input/output flag pins	Enable sophisticated automation setups and camera test stations; enable output flag programming based on arbitrary trigger events
<b>User Interface</b>	Introspect ESP GUI allows for interoperation with embedded instruments, FPGA instruments, and other lab tools	Enables full lab automation; provides a scalable, future-proof solution
<b>Scripting</b>	Data logging; automatic report generation	Suited for performing full conformance testing

## Detailed Analysis Capability

The screenshot displays the DPHY Data Capture software interface with several key features highlighted:

- Capture summary:** A table showing captured data with columns for ID, Time (ms), VC, Index, DT, DT Name, ImageWidth, ImageHeight, FirstPacket, and LastPacket.
 

ID	Time (ms)	VC	Index	DT	DT Name	ImageWidth	ImageHeight	FirstPacket	LastPacket
0	0.000225	0	0	0x24	RGB888	1080	720	0	221
1	50.000307	0	1	0x24	RGB888	750	1334	222	2057
2	190.000389	0	2	0x24	RGB888	1440	1080	2058	3135
3	150.000475	0	3	0x24	RGB888	1080	720	3140	3881
4	200.000557	0	4	0x24	RGB888	750	1334	3882	5197
5	250.000638	0	5	0x24	RGB888	1440			
- Images automatically reconstructed and saved:** A window showing a reconstructed image of a building.
- Precision time stamps:** A table showing detailed packet information with columns for Packet ID, Time (ms), Burst, DT, DT name, Header ECC, WC, Payload CRC, and Short.
 

Packet ID	Time (ms)	Burst	DT	DT name	Header ECC	WC	Payload CRC	Short
0	0.000225	0	0	FrameStart	0x00			0x0000
1	0.000307	1	0	0x24	0x34	0x00	0x0000	
2	0.000326	2	0	0x24	RGB888	0x34	3240	0x28E5
3	0.000326	3	0	0x24	RGB888	0x34	3240	
4	0.090221	4	0	0x24	RGB888	0x34	3240	0xAE51
5	0.130321	5	0	0x24	RGB888	0x34	3240	0x62C3
- Short and long packets are automatically enumerated, header details extracted:** A detailed view of a packet showing its structure and data.
- Errors highlighted:** Red markers in the packet details view indicating detected errors.
- Hyperlinks for navigating between common bits, bytes and frames:** A navigation pane with buttons for 'bits', 'bytes', and 'frames'.
- Bytes from each lane before and after being merged:** A table showing data for lane1, lane2, and lane3.
 

	0	1	2	3	4	5	6	7	8	9	10	11	12
lane1 data:	24	2C	66	66	66	E6	E6	E6	36	76	76	86	76
lane2 data:	15	37	37	57	D7	97	97	97	D7	D7	D7	D7	77
lane3 data:	30	D5	D5	35	B5	B5	B5	35	75	0D	75	75	8D
bytes:	248B0C	84E2A8	6EE2A8	66...	6EE2AD	67E9AD	67E9AD	67E9AC	6CEBAE	6EECB0	6EEBAF	6DEBAE	6EEEBE
- HS bits, per lane, automatically translated to hex and decimal:** A window showing the raw bitstream and its conversion to hexadecimal and decimal values.