

Generating an External Trigger from the SV3C-DPRX MIPI D-PHY Analyzer

Technical Insights

External Triggering on the SV3C-DPRX

It is useful at times to generate or receive an external LVCMOS trigger on a pin when using the SV3C-DPRX MIPI D-PHY Analyzer. This could be used to trigger external equipment such as an oscilloscope or internal debug equipment/probe to start a debug sequence from a pin on a payload error. For example, when analyzing very long traces from a device under test, an active probe can be placed on the signal being analyzed and exported to an oscilloscope. Then, if the SV3C-DPRX analyzer captures an error event, it in turn generates a trigger to the oscilloscope so that it can freeze the signal waveform that led to the error. Alternatively, the SV3C-DPRX analyzer can be armed to receive an external trigger for it to start its own capture. This capture, for example, could be synchronized to external timing events that are generated within the larger context of entire-system operation. This may be extended to other applications or examples.

EXTERNAL TRIGGER OUTPUT

Generating an external trigger output based on a capture event is very easy to do with the SV3C-DPRX DPHY analyzer. When you set up your capture on the analyzer, you must select a trigger as shown in **Figure 1** below:

| Components | csiDataCapture 1 properties (class: MpiDphyCsiDataCapture) | |
|---|---|---|
| cs0btACpture1 LuncList mpCheckConfig1 mipiProtocol | InneList Lanes capture/Mode taggerCondition preTinggerCuration potTinggerCuration potTinggerCuration caliFawFormatBayerCell timeout caliFpd war4-halytis imageFileFormat war4PixeIDataFiles savePieuits | |
| Add Remove Config | "triggerCondition" is "anyBurst", the capture will be tr | iggered by the start of an HS burst. If "triggerCondition" is "ipSequence", the capture will be triggered by the LP states specified in the p |



When this trigger condition is met, pin 5 on the 12-pin header connector of the unit will be asserted at the same time your data capture starts. The header is numbered from right to left as in the diagram (**Figure 2**) on the following page.



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Pin 5 will remain asserted until a new test is triggered, for example by pressing 'Run' in the GUI.

When captured on a scope, you can see GPIO 5 gets asserted (the red trace which goes high in **Figure 3**) after the frame start is received (the two short packets shown in the yellow trace in **Figure 3**).





EXTERNAL TRIGGER INPUT

In order to use an external signal to trigger a capture on the SV3C-DPRX D-PHY Analyzer, you need to use a low level command to override the normal trigger action and set the analyzer to trigger on a signal sent to GPIO pin 6 (shown in **Figure 2**). The trigger should be a LVCMOS signal with a nominal level of 2.5V.

Here is a simple example:

iesp=getlespInstance() #Required to run low level commands mipiClockConfig1.setup() iesp.setTriggerOverride(True) #Tells the analyzer to capture on a signal on pin 6 csiDataCapture1.run() #Start the capture and wait for the trigger



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CONCLUSION

In this short Technical Insights brief, we illustrated how easy it is to both generate or receive external triggers on the SV3C-DPRX MIPI D-PHY Analyzer. This feature is a powerful debug aid to capture the insights you often require during design validation.