PRODUCT BRIEF

M SERIES

SV7M-LPDDR5PA
LPDDR5 Protocol Analyzer

High-Performance Debug, Compliance Validation, and Analysis

The SV7M-LPDDR5PA is a complete solution for validating and debugging LPDDR5/LPDDR5x memory interfaces. Providing support for one complete channel of an LPDDR5 DRAM (covering both the command and data buses), this analyzer can capture read and write commands, and it can provide deep analysis of all protocol events on the LPDDR5 bus. Coupled with interposer systems based on high-impedance active probing, this analyzer is capable of measuring new LPDDR5/LPDDR5x systems running at 8533 MT/s or more.

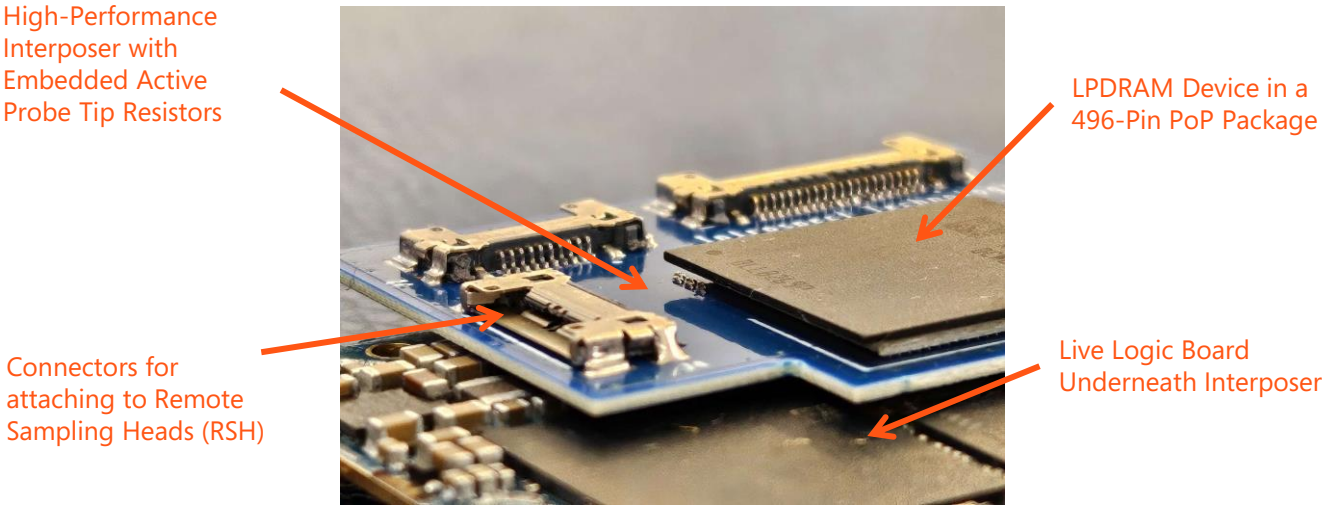
KEY FEATURES:

- **Modular Design:** Remote sampling heads (RSH) are placed close to the device under test (DUT)
- **Active Probe Technology:** RSHs contain 10 GHz bandwidth active probes for all 32 channels
- **Multi-Protocol DDR Command Capture:** Supports decoding and analysis for LPDDR4, LPDDR5, LPDDR5x, and DDR5
- **Triggered Digital Capture:** One-shot triggering on command and capture data bus in parallel

KEY BENEFITS:

- **Complete Data and Command Capture:** Modular design allows scaling to numerous simultaneous capture channels
- **Superior Signal Integrity:** Active probing results in high-bandwidth measurement and easier de-embedding of interposer losses
- **Easy Debug:** Electrical and protocol validation testing can occur with the same interposers and the same RSH active probe technology

Typical Application: Package-on-Package Probing of Live Systems

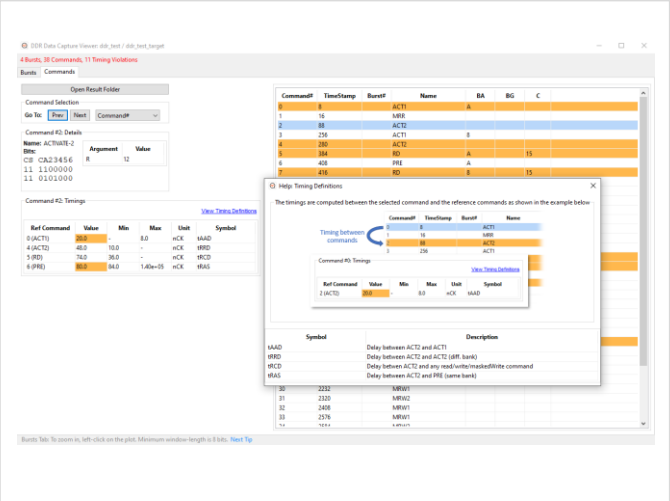


Introspect Technology's LPDDR5 Interposer Solution

Specifications

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Ports			
Number of differential (or single-ended) receivers	32		The SV7M-LPDDR5PA covers an entire channel of a LPDDR5 device (consisting of the command bus and the 16 data pins)
Number of GPIO Pins	12		Used to automatically calibrate all remote sampling heads
Connections to PC for Pinetree software control	2		USB Type-C
LPDDR5 Specifications			
Command triggers	Any		Can trigger on ACT1, ACT2, CAS, DES, MPC, and all commands in the LPDDR5 truth table
Maximum transfer rate	8700	MT/s	Higher rates can be captured with limitations
On-board memory	16	Gbyte	
Electrical Specifications			
Input common mode range	50-1000	mV	Covers LPDDR5 and DDR5 applications
Skew resolution	5	ps	Provides high-accuracy shmoo capability
Voltage resolution	10	mV	Provides high-accuracy shmoo capability

Detailed Compliance Checks on Command and Address Bus



Command View With Timing Parameter Measurements

Data Bus Burst View With Waveform Display