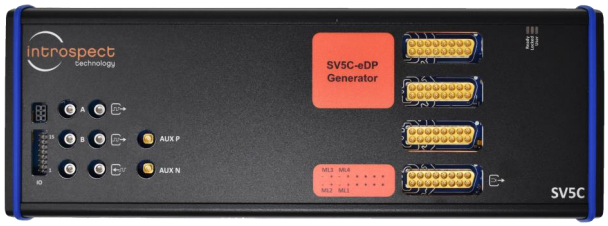
C-SERIES

SV5C-eDP Generator

Embedded DisplayPort Generator



High-performance generator for eDP v1.5 and DP v2.1 systems in HBR

The SV5C-eDP Embedded DisplayPort Generator is an ultra-portable, high-performance instrument capable of generating traffic for Embedded DisplayPort and DisplayPort applications at data rates of up to 12.5 Gbps. The SV5C-eDP Generator provides analog parameter controls that enable DisplayPort receiver stress-testing and allow for deep insights into voltage and timing sensitivities of DisplayPort sink devices. The instrument operates with Introspect Technology's award-winning software, Pinetree, which includes full pattern synthesis tools for generating test patterns and video frames for system-level test.

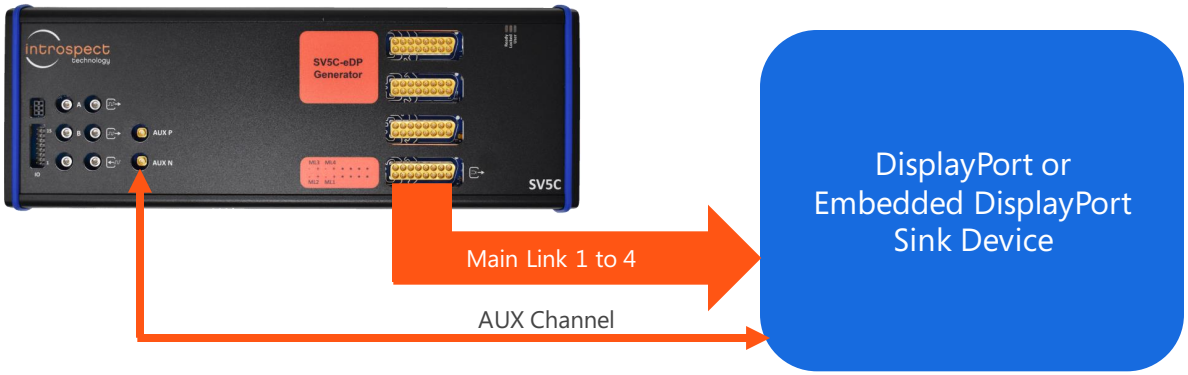
KEY FEATURES:

- **Protocol:** supports Embedded DisplayPort up to v1.5 and DisplayPort up to v2.1 in HBR
- **Supported Data Rates:** up to 12.5 Gbps with a fully continuous range of data rates
- **Lane Count:** configurable from 1 to 4 lanes per port plus Auxiliary Channel
- **Pattern Generation:** full video frame generation with 2 GBytes of pattern memory

KEY BENEFITS:

- **Analog controls and signal impairments:** unique features for stressing a DisplayPort sink device, including per-lane voltage amplitude, common-mode voltage control, jitter injection, sinusoidal voltage noise injection, and per-wire timing skew
- **Self-Contained**: an all-in-one system that enables the simplest bench environment for physical layer test to full protocol layer validation
- **Automated:** leverages the full power of Python and Introspect's award-winning software environment, Pinetree

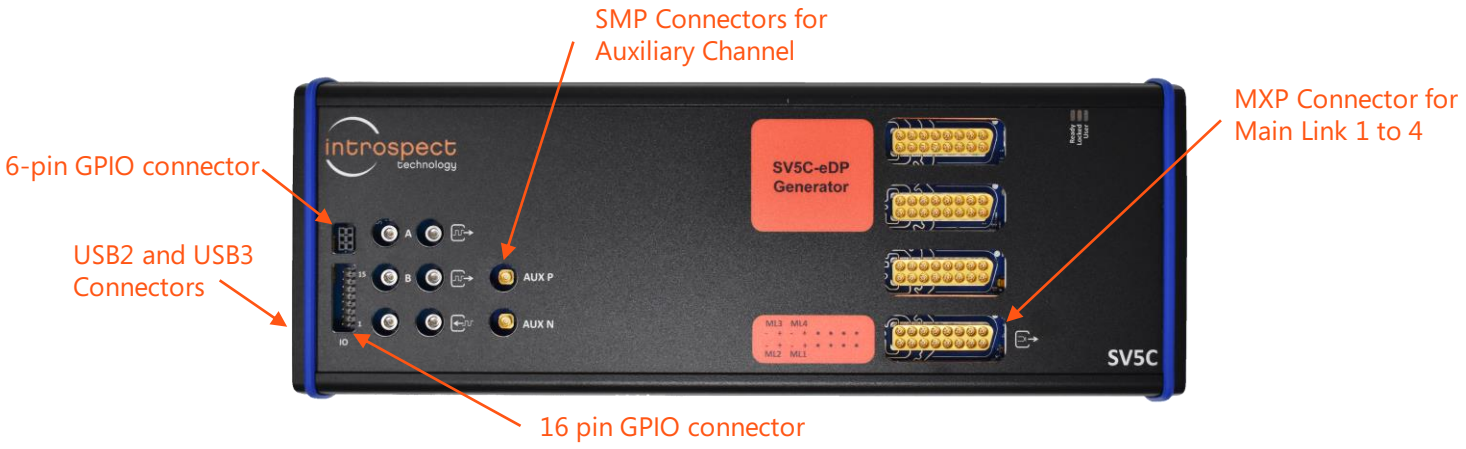
Typical Application: The SV5C-eDP Generator transmitting video to a DisplayPort sink device



GENERAL SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION
Application/Protocol			
Physical Layer Interface	eDP and DP		Support for eDP to version 1.5 Support for DP to version 2.1 in HBR
Ports			
Number of Transmitter Lanes	5		Main Link 1, 2, 3, 4 AUX Channel (bidirectional)
Number of GPIO pins	5		Programmable as external trigger input or flag output pins
Number of dedicated reference clock inputs	1		
Number of dedicated reference clock outputs	2		
PC connections for Pinetree control	2		USB2 and USB3
Data Rates and Reference Clocks			
Minimum Data Rate	1562.6	Mbps	Per Lane
Maximum Data Rate	12.5	Gbps	Per Lane
Minimum External Input Ref Clock	10	MHz	
Maximum External Input Ref Clock	250	MHz	
Minimum External Output Ref	10	MHz	
Maximum External Output Ref	500	MHz	

Physical Connections of the SV5C-eDP Generator



The SV5C-eDP Generator's lanes (main link 1 to 4) are contained on a single MXP connector.