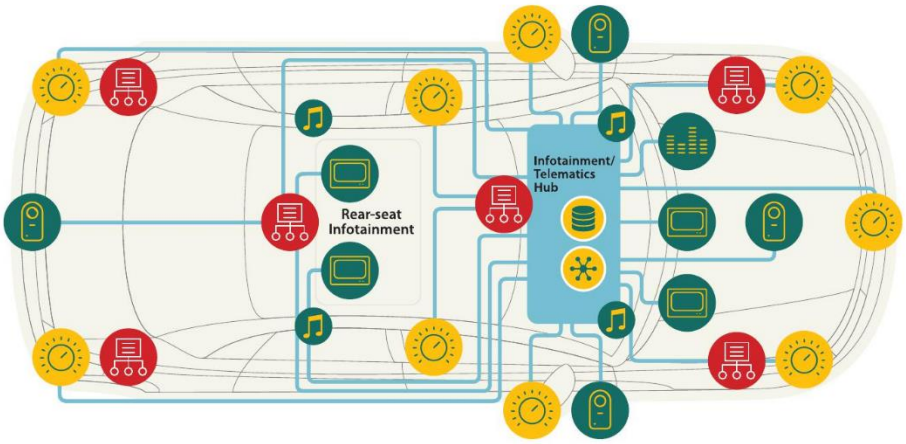
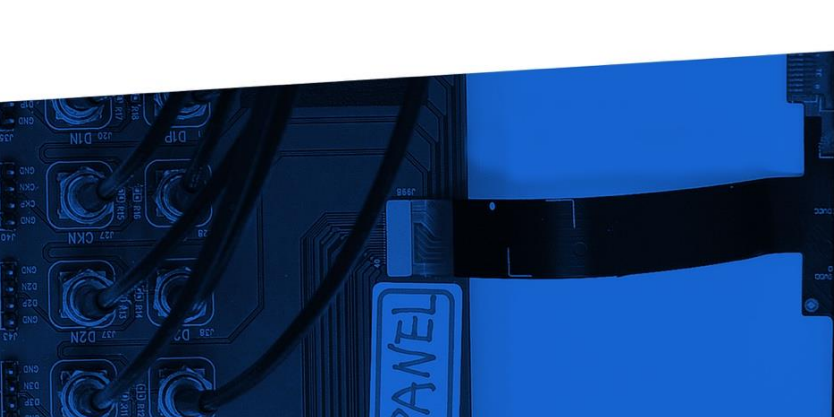
introspect technology

WHITE PAPER

MIPI Testing in ADAS

SERIES NAME





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Introduction

OVERVIEW

Over the last few years, growing concerns about automotive safety among consumers has resulted in high demand for advanced safety features, and as a direct result, car manufacturers and industry analysts are predicting an increase in demand of over 25% for ADAS-equipped automobiles by the year 2020.

Advanced driver assistance systems (ADAS) applications contribute to a safer environment for everyone sharing our roadways: drivers, passengers, and pedestrians alike. ADAS applications provide additional information about the surroundings of the car to the driver through surround view or rear-view systems and can warn the driver of dangerous situations through lane departure and blind spot warnings. This is accomplished by using an increasing number of data sources via sensors installed around the entire perimeter of the vehicle.

These data sources are typically connected to an Infotainment Telematics Hub via a Network Bridge which incorporates a MIPI to/from Auto SerDes translator. The Auto SerDes link provides power and control data to the sensors, but its main function is to drive high-speed data over the long length channels found in most automotive cable harness assemblies.

In this paper, we describe an Auto SerDes implementation based on an FPD link solution from Texas Instruments, and the concepts here are applicable to any Auto SerDes technology such as Apix-3 from Inova Semiconductor or SerDes solutions from Maxim Integrated to name a few.

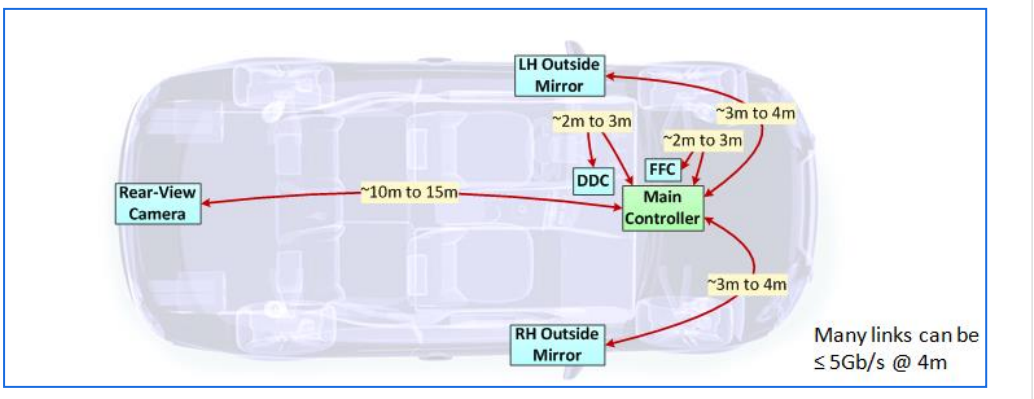

Figure 1: Auto SerDes links are used in ADAS systems to drive long cables (Source: MIPI Alliance)

FPD-LINK

FPD-Link is the original high-speed digital video interface created in 1996 by National Semiconductor (now within Texas Instruments). It is a free and open standard for connecting the output from a graphics processing unit to the display panel's timing controller.

Automotive infotainment displays for navigation systems started using FPD-Link in 2001. BMW was the first car maker to use FPD-Link in their cars for transferring navigation graphics from the head unit to the central information display. Many other car manufacturers then started using FPD-Link. Today, most infotainment and driver assistance applications are using FPD-Link II and FPD-Link III to benefit from the embedded clock and control signals. One of the main benefits is the reduced cable size and weight due to the single wire pair for all the data and clock signals. (Source: https://en.wikipedia.org/wiki/FPD-Link)

ADAS SUB-SYSTEM

This document describes how *Introspect* DPHY test tools can be employed in testing such ADAS/FPD-Link systems. More specifically, we will be describing a commercial FPD-Link III sub-system, its interfaces, and how we can test them.

The FPD-Link III sub-system that we will be interfacing to is shown in the block diagram that follows.

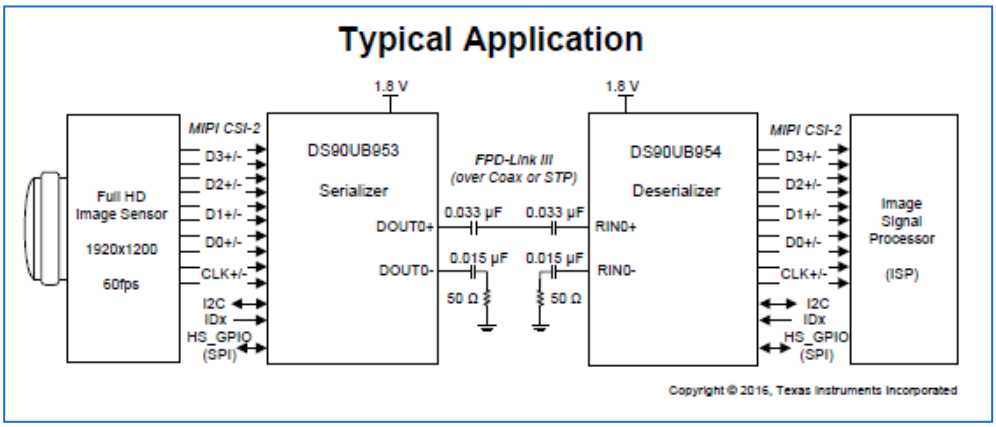

Figure 2: FPD-Link III sub-system under test Block diagram

As shown in the Block diagram, the FPD-Link III interface is at the center of the sub-system, but the inputs and outputs of the sub-system are both MIPI-CSI interfaces. MIPI technology is a favorable component choice for car manufacturers as it allows them to leverage low-cost, high-performance image sensors and processors from the mobile phone industry.

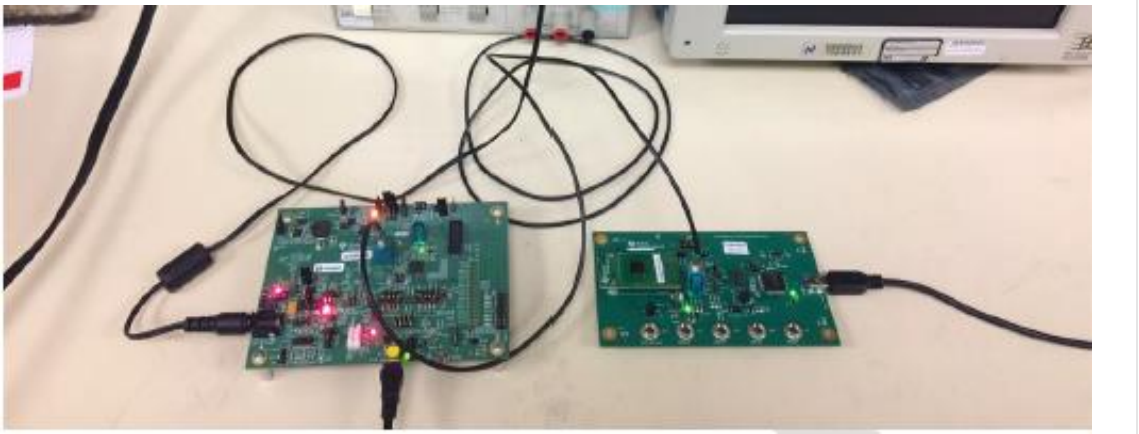

Figure 3: FPD-Link III sub-system under test (DUT)

To prove that the sub-system is fully operational, a MIPI CSI-2 stimulus is applied at the input of the sub-system and then the MIPI CSI-2 output from the sub-system is captured and analyzed (or processed by a MIPI receiving device).

This stimulus can come from multiple sources:

- Commercial Image Sensor (as shown in Figure 3)
- Introspect SV3C-DPTX MIPI DPHY Generator

The output can be captured and analyzed (or processed) using the following devices:

- Commercial MIPI CSI-2 Receiver
- Introspect SV3C-DPRX MIPI DPHY Analyzer

Test Scenarios

This section describes various testing scenarios.

SCENARIO #1: LIVE LINK TEST

This test demonstrates how we can use the combination of Introspect PV1 Probes and a DPHY Analyzer to sniff the MIPI CSI-2 bus and perform packet data analysis without disrupting the live link. Several MIPI bus timing parameters are also extracted to validate conformance to specifications.

A block diagram of the Live Link Test hardware setup is shown below.

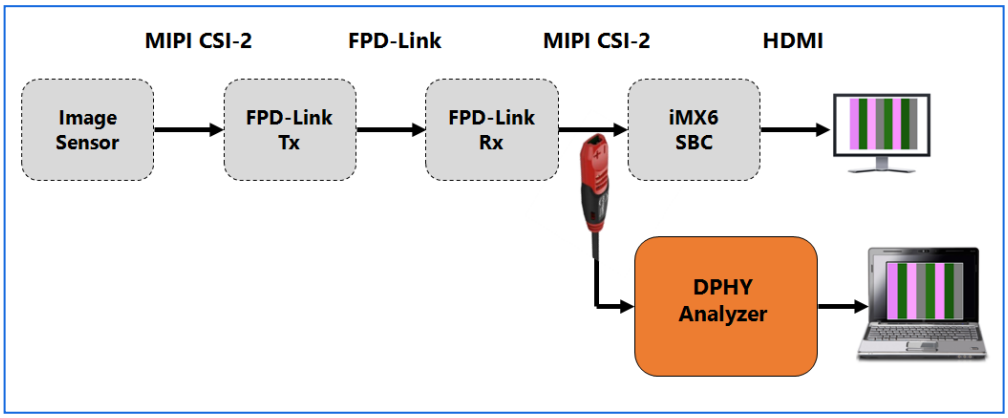

Figure 4: Live Link Test Block Diagram

The Live Link Test hardware is composed of the following components:

- **Image Sensor:** Omnivision OV10640 installed on a daughter card and inserted into FPD-Link MIPI Input connector
- **FPD-Link Tx:** Texas Instruments DS90UB953EVM
- **FPD-Link Rx:** Texas Instruments DS90UB954EVM
- **iMX6 SBC:** A commercially available Single-Board Computer (SBC) containing a Freescale iMX6 application processor
- **Probes:** Introspect Technology PV1 Active Probe

- **DPHY Analyzer:** Introspect Technology SV3C-DPRX
- **Commercial Laptop:** Any brand, running a Microsoft operating system

In this test, the sub-system is setup in normal operation, where a MIPI source transmits a stream of images through the FPD-Link sub-system. The sub-system MIPI output is sent to a commercial SBC where the received images are displayed on a commercial HDMI display.

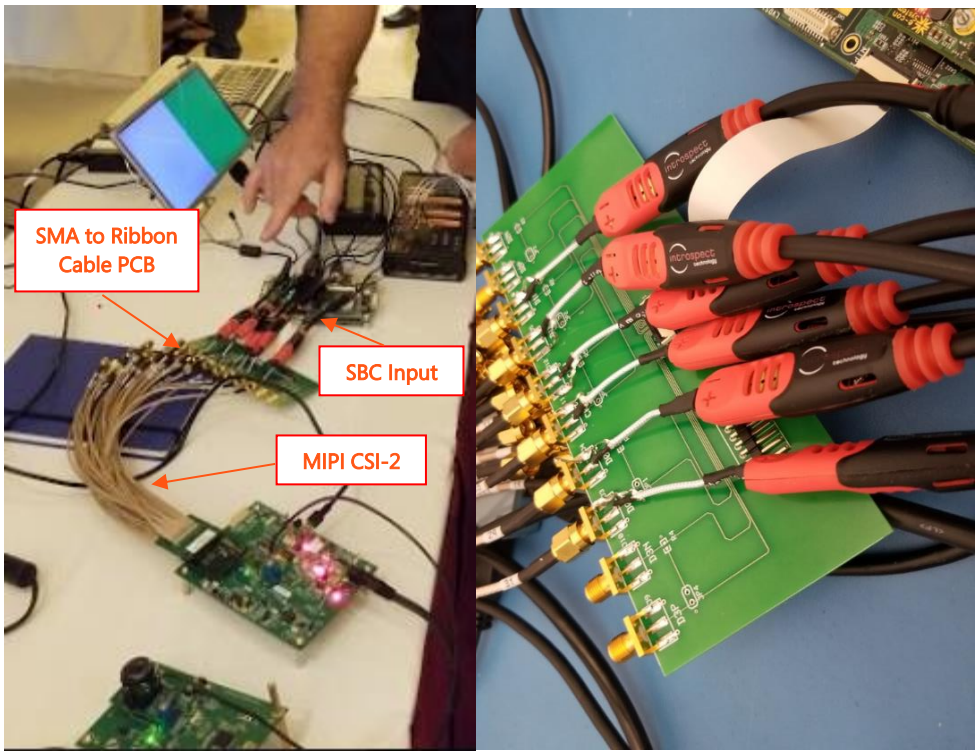

Figure 5: Photo of Live Link showing probe insertion at input of SBC

In the photo for **Error! Reference source not found.**, a PCB is used to convert the MIPI CSI-2 Output from SMA cable to Ribbon cable as required for the SBC input. The probes are installed at this location. It is recommended to install the probes as close as possible to the MIPI Receiver input.

SCENARIO #2: IMAGE CAPTURE TEST

This test demonstrates how the Introspect DPHY Analyzer can be used as the endpoint which receives the sub-system MIPI output. The endpoint performs dynamic termination control as per MIPI specifications, and then captures image data from the sub-system based on flexible trigger mechanisms. Analysis is performed on every packet, showing errors where applicable. Received images are reconstructed for viewing.

A block diagram of the hardware setup is shown below.

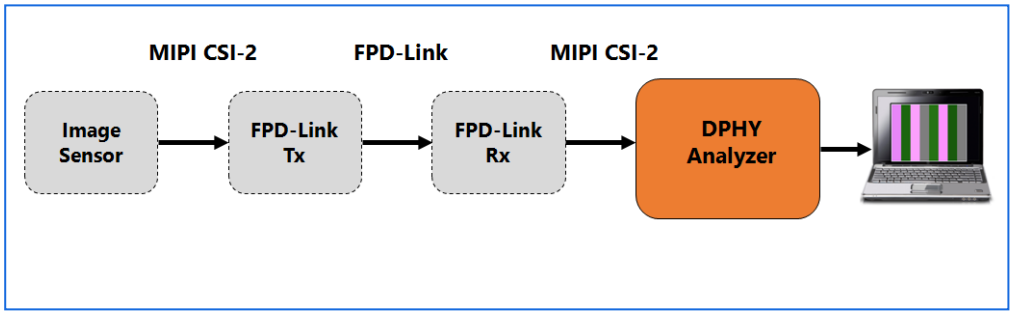

Figure 6: Image Capture Test Block Diagram

SCENARIO #3: IMAGE GENERATOR TEST

This test setup shows how the *Introspect DPHY Generator* can be used to stress the sub-system MIPI input. Stress sources can be voltage amplitude attenuation, clock to data skew, injection of controlled amounts of jitter, MIPI global timing parameter violations, invalid SOT marker, and so on. Functional tests can also be performed to test different image formats, frame rates, frame numbering, line rates, line numbering, blanking, encryption, and so on.

A block diagram of the hardware setup is shown below.

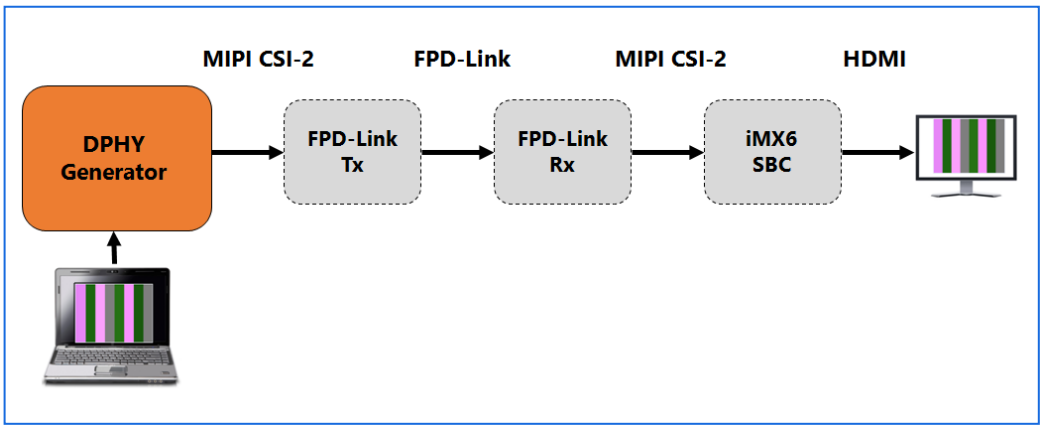

Figure 7: Image Capture Test Block Diagram

In this block diagram, a new component is introduced which emulates the MIPI CSI Image Sensor.

- **DPHY Generator:** Introspect Technology SV3C-DPTX

Test Execution & Results

In this section, we describe software setup and test results from the different testing scenarios.

SCENARIOS #1 & 2: DPHY ANALYZER

Example1: Frame Capture

The Introspect DPHY Analyzer is set up to capture full frames as follows.

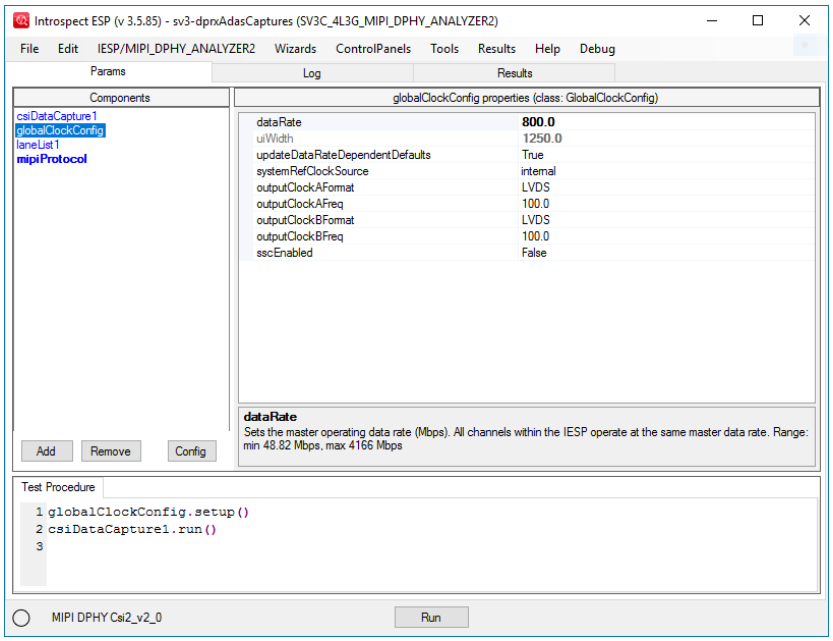

Figure 8: Data Rate Setup

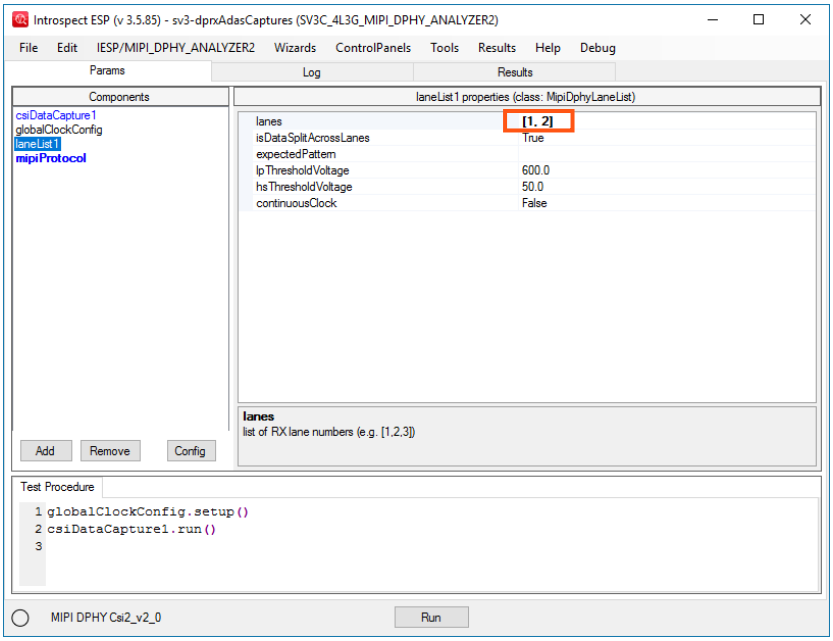

Figure 9: Number of Lanes setup

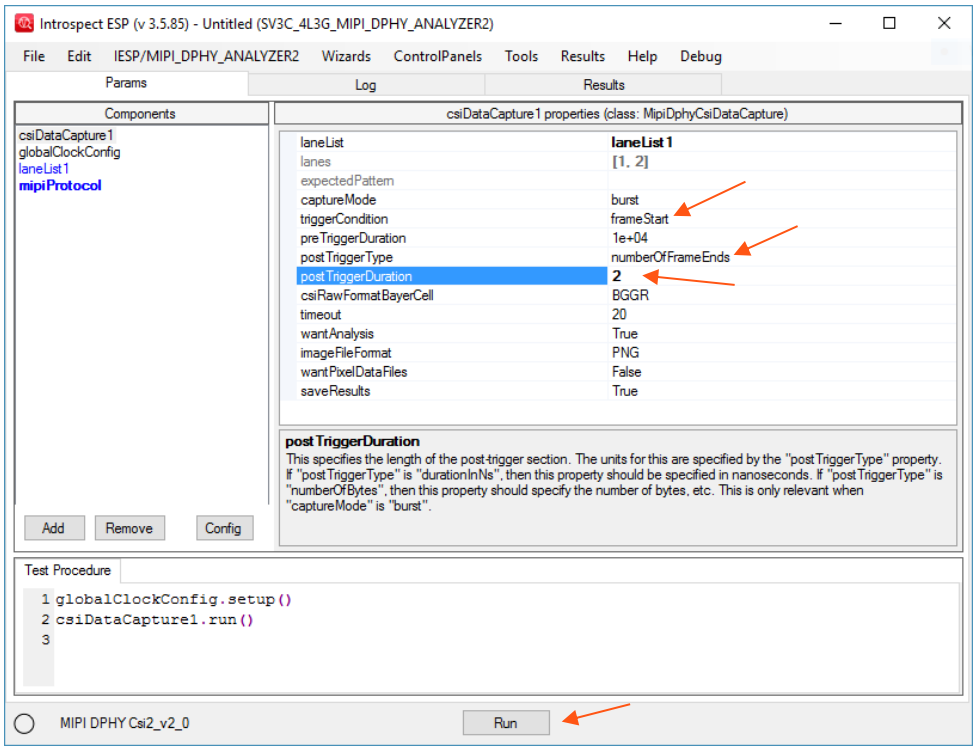

Figure 10: Trigger setup for capturing 2 full frames

To run a test, the operator assigns component properties and then presses the Run button.

Analysis Results

When the capture runs without error, it is most interesting to look at the 'Frames' view, which presents a high-level summary of the captured image properties.

The following screenshot shows the reconstructed image. No errors were found in the 'HS Bursts', 'CSI Packets', 'LP States', and 'LP Events' analysis views.

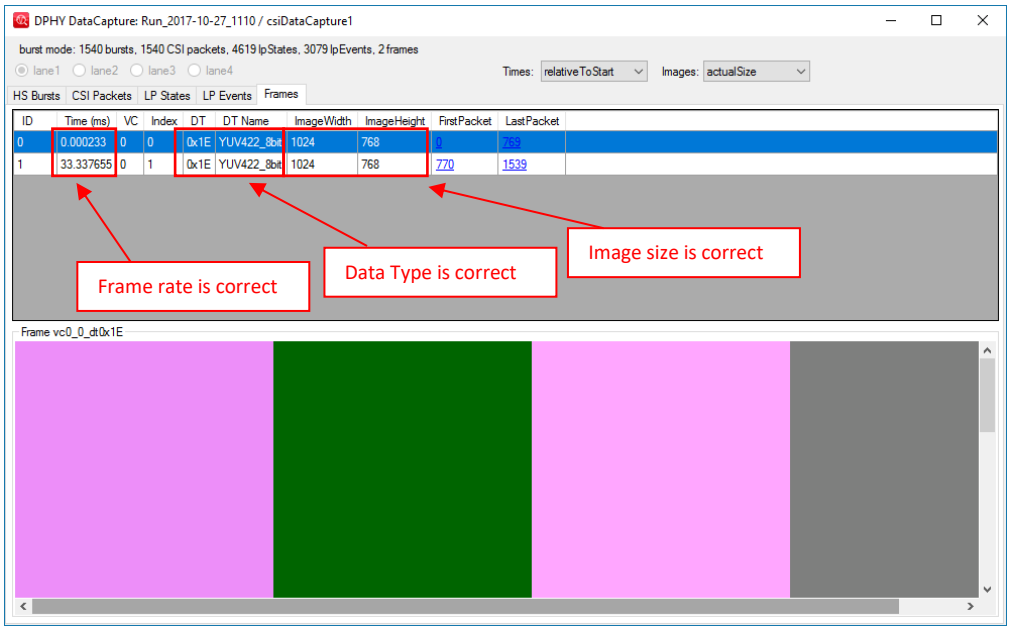

Figure 11: Two full frames captured without error

Frame View

In the above Frame Capture, the expected image size was 1024x768 and the expected image format was YUV422 (8bit). The Image Sensor was transmitting a color bar pattern at a frame rate of 30fps (period=33.33ms). There were no errors in the captured Bursts or Packets. This capture reveals that the link was functioning correctly.

Example2: Burst Capture

When errors are present in the Frame capture, or when a Frame capture is not possible, it is more useful to perform Burst captures. This example shows how burst captures can be used to debug a faulty system.

The following screenshots show how the *Introspect DPHY Analyzer* is set up to capture bursts of data. A burst is defined as a transition out of the low power

Stop state and into the High-Speed Data Transfer state and then back to the low power Stop state.

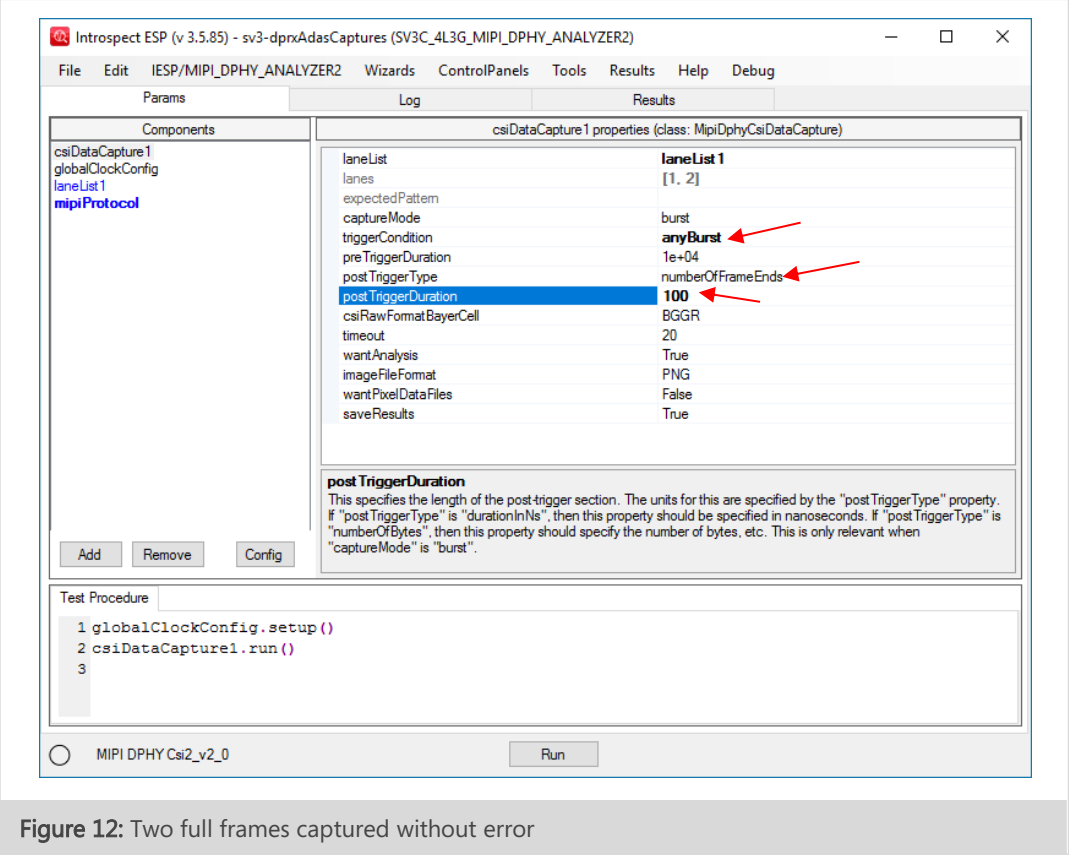

Figure 12: Two full frames captured without error

Analysis Results

The first result below shows a burst mode capture of 100 bursts. The report shows that there were errors in some of the bursts/packets. Despite the presence of errors, the software attempts to reconstruct the received image based on valid data received.

To debug this scenario, we can leverage the selection of views provided by the analysis software.

First, we look at the 'LP States' view. Here we see valid transitions from the Stop state (LP11) to HS-Request state (LP01) to HS-Prepare state (LP00). From the time column, we can see the global timing parameter TLPX = 60ns (time spent in LP01 state), which is within specifications. We can also observe that the sequence (LP11-LP01-LP00) timing is repetitive, which is expected behavior during a frame

transmission as this is the line timing. From the line timing, one can separate active pixel time (LP00) from blanking time (LP11).

We conclude that the problem is not LP related.

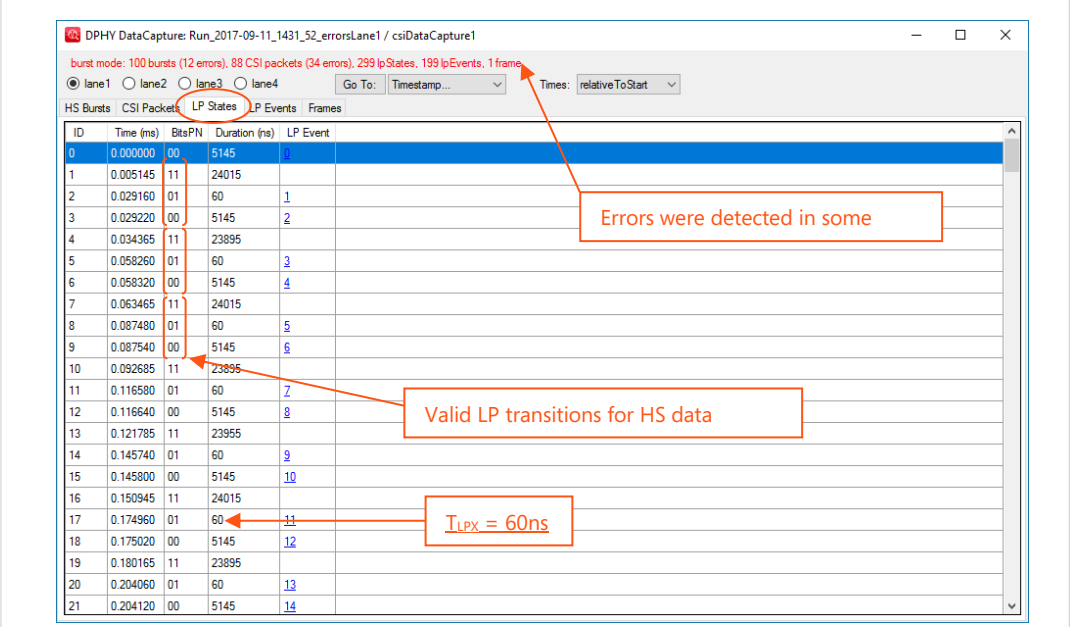

Figure 13: Analysis of LP state transitions

Next, we look at the HS activity by selecting 'HS Bursts' view. This view shows some red cells (bursts with errors) and some normal cells. We will look at both cases below.

Burst With No Errors

Burst #26 shows a normal capture where all PHY-level events are without error. An SOT marker was detected, and the number of bytes that follow are counted and stored for further analysis.

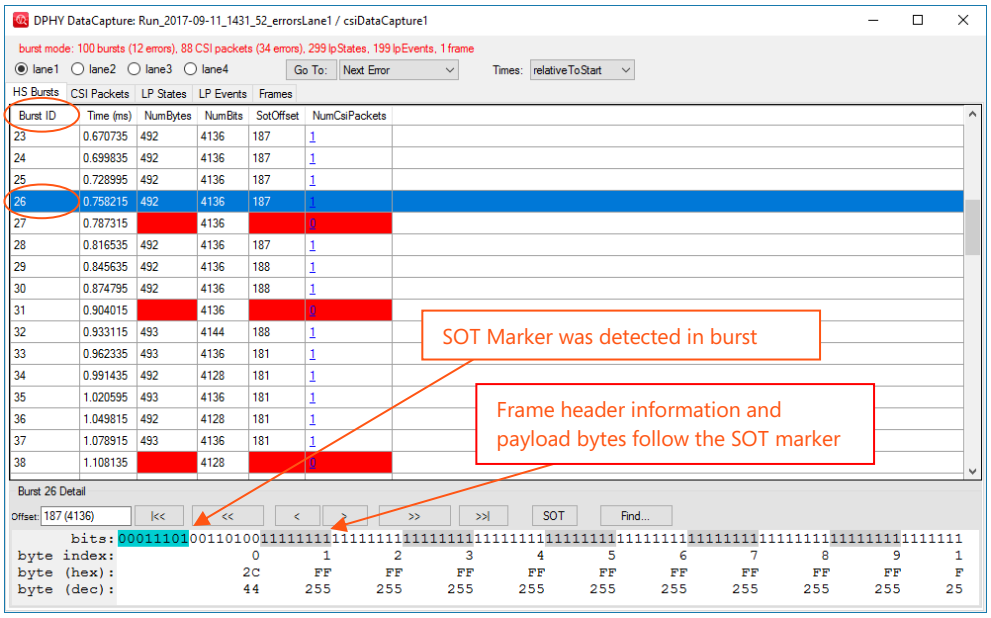

Figure 14: Analysis of burst #26 showing an SOT marker followed by bytes (no errors in this burst)

Burst With Errors

In burst #27, no SOT marker was found during the analysis (clicking on the SOT button yields no results), therefore NumBytes and SotOffset cannot be determined. This burst can not be used to form a CSI packet, and therefore we expect some lines will be missing in the reconstructed image. All bits captured on this lane can be viewed in the "bits" field in the lower window. You can use the "Find..." button to search for any bit combination in the bitstream.

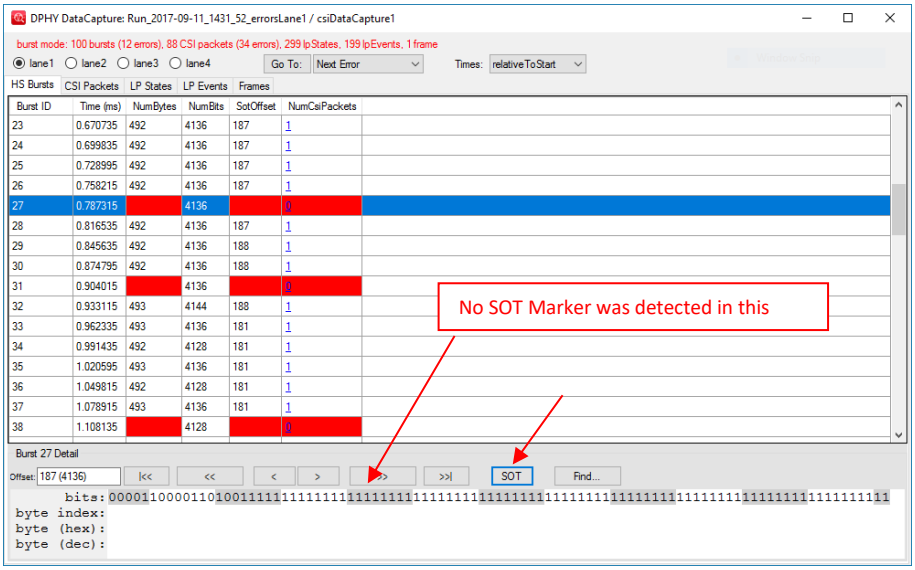

Figure 15: Analysis of burst #27 indicating errors were detected

Packet View

Next, we move up a level to the 'CSI Packets' view. This view also shows some errors (red cells).

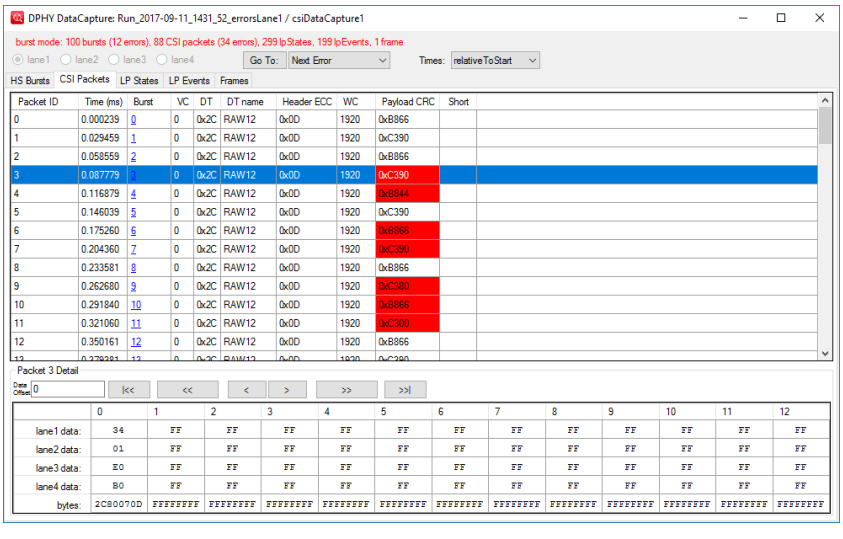

Figure 16: CSI Packets View

CSI Packets are constructed by merging valid HS Burst data from all lanes. The packet header is analyzed and key parameters such as Virtual Channel (VC), Data Type (DT), and Word Count (WC) are extracted and presented. When the ECC field in the packet header or the CRC field in the packet payload does not match with the value computed by the Analyzer, an error is flagged (highlighted in red).

Frame View

Finally, we can move up one more level to the 'Frames' view. Frames are constructed by merging valid CSI Packets, usually delimited by 'Frame Start' and 'Frame End' packets.

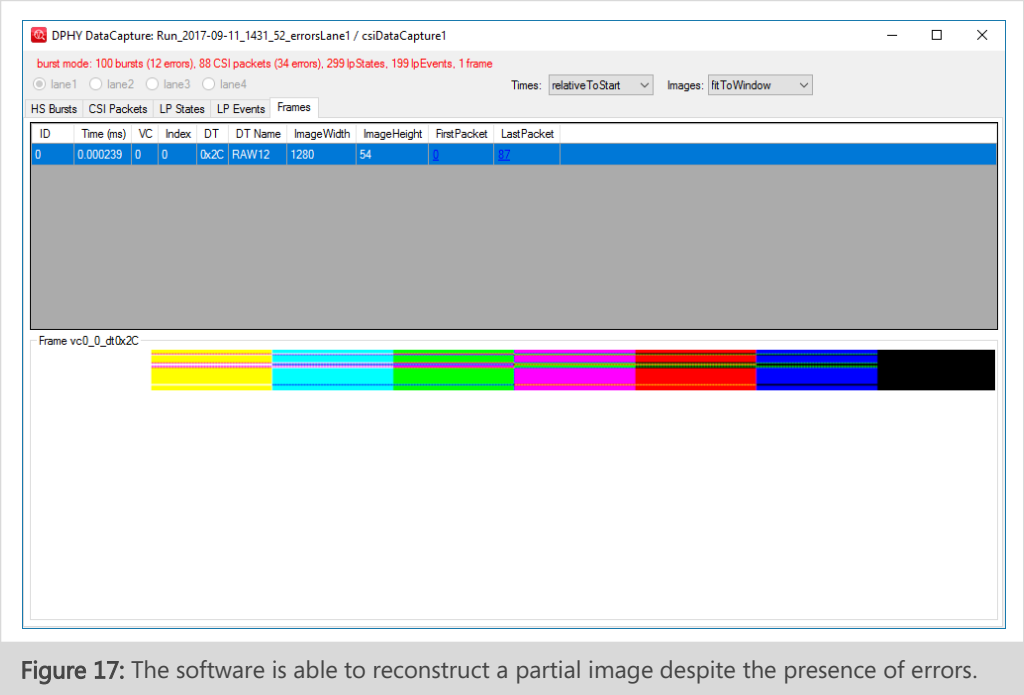

Figure 17: The software is able to reconstruct a partial image despite the presence of errors.

In the Frames view, we see the reconstructed image. We can observe an image width of 1280 pixels (which is correct) and a height of 54 lines (partial image). The image is partial because we limited the capture to 100 bursts and some bursts/packets had errors. Despite the errors, we can see that the image is what we are expecting (i.e. a color bar image), which is encouraging.

Later in the debugging process, it was found that an intermittent connection was the source of the CRC errors in the packet view and the missing lines in the frame view. The SV3C-DPRX was indispensable in rapidly pinpointing the source of the issue and ruling out any protocol or global timing errors.

SCENARIO #3: DPHY GENERATOR

The following screenshots show how the Introspect DPHY Generator can be set up to emulate the same Image Sensor.

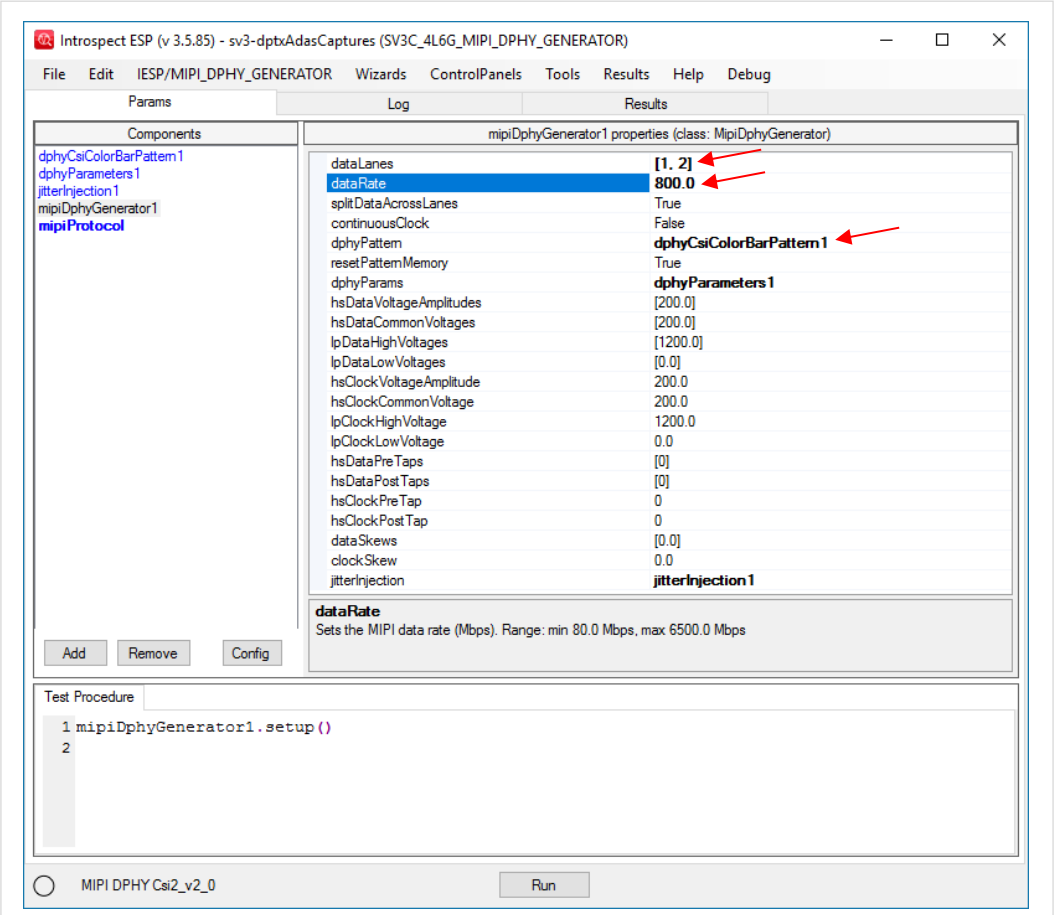

Figure 18: Set up for color bar image transfer on 2 lanes at 800Mbps

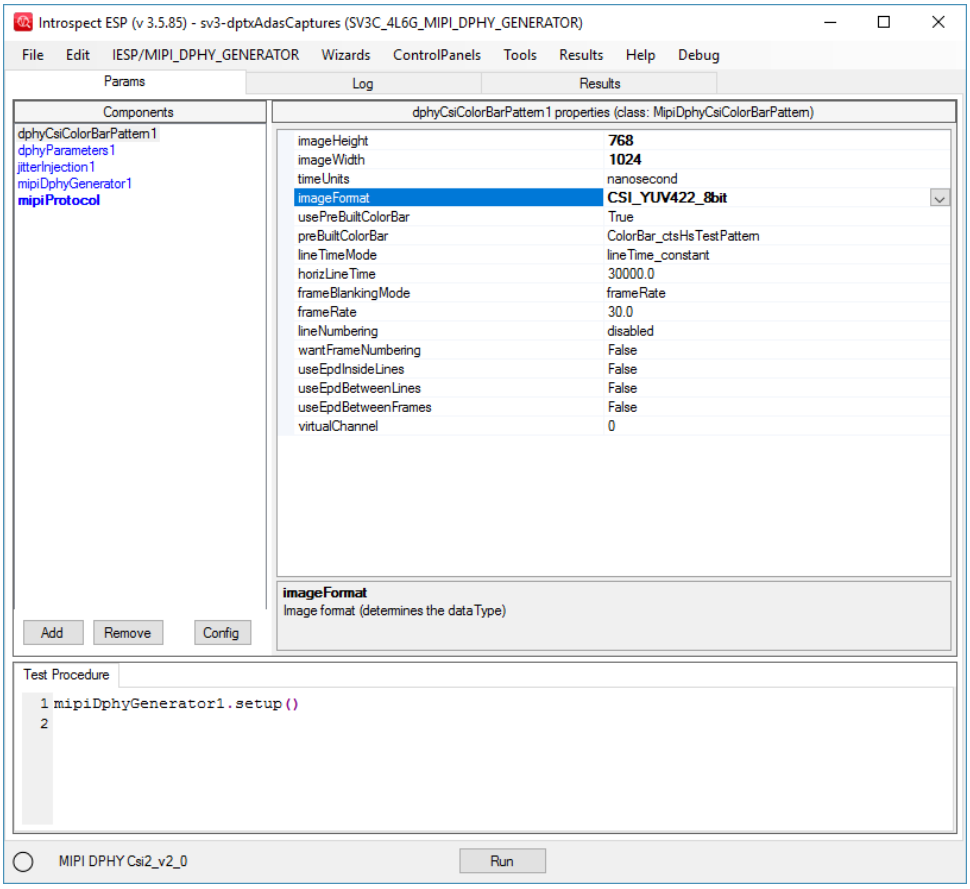

Figure 19: Set up for color bar image properties

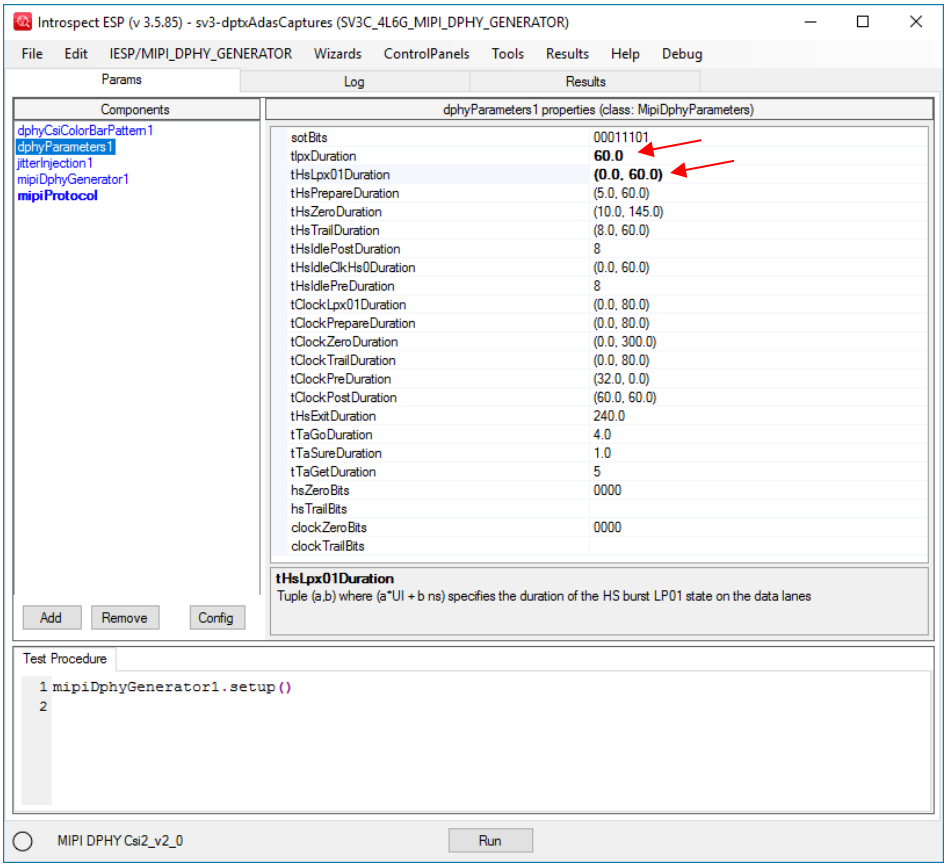

Figure 20: Setup for MIPI global timing parameters

The process is quite simple, after all properties are setup, the operator presses the 'Run' button and the image is transferred continuously.

Default values are always valid and within specifications. These can be used for testing with nominal conditions. The values can be changed to best-case, worst-case, or even out-of-spec values for stress testing any MIPI CSI-2 Receiver.

For higher data rates, a jitter injection component and calibration burst can be enabled as well.

Conclusion

This paper described an Automotive SerDes link and how it interfaces to electronic processing components using MIPI conduits. We also showed an end-to-end testing scheme for such SerDes link, deploying Introspect generators and analyzers to respectively stress receiver electrical parameters and analyze transmitter protocol and physical layer behavior. We illustrated the use of active probes to monitor live traffic, and we also demonstrated the use of Introspect analyzers as terminating endpoints, featuring fully integrated switchable termination resistors as per the MIPI Alliance specifications.

For more information about development, verification, and production instruments and equipment for SerDes and MIPI applications, visit the Introspect Technology website, www.introspect.ca, and our resources page at www.introspect.ca/resource-center

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1.2	Updated format	December 20, 2022

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