

Jitter Transfer Functions in Minutes

In this paper, we use the **SV1C Personalized SerDes Tester** to rapidly develop and execute PLL Jitter transfer function measurements. We leverage the integrated nature of the tool and its automation features to develop tests, execute scripts, and generate automatic reports in minutes.

The paper is organized as follows. The definition of jitter transfer and its relevance to high-speed standards is first presented. We then describe the measurement concept used in this paper and construct a very simple **Introspect ESP Test Procedure** for the automatic collection of PLL jitter transfer functions and loop bandwidth parameters. We then describe advanced topics related to min-max VCO testing, time-domain testing, and linearity.

Why Measure the Jitter Transfer Function?

Figure 1 shows a typical high-speed serial link as described in [1]. As can be seen in this PCI Express example, multiple phase-locked loop (PLL) circuits exist in both the transmitter and the receiver. These circuits are critical in order to ensure error-free operation at very high data rates (e.g. 8 Gbps) while using relatively inexpensive clocking topologies. When viewed in the “phase domain”, these phase locked loops essentially behave as frequency selective filters (H_1 , H_2 , and H_3 in the figure), passing certain frequency bands of “phase” and rejecting other frequency bands.

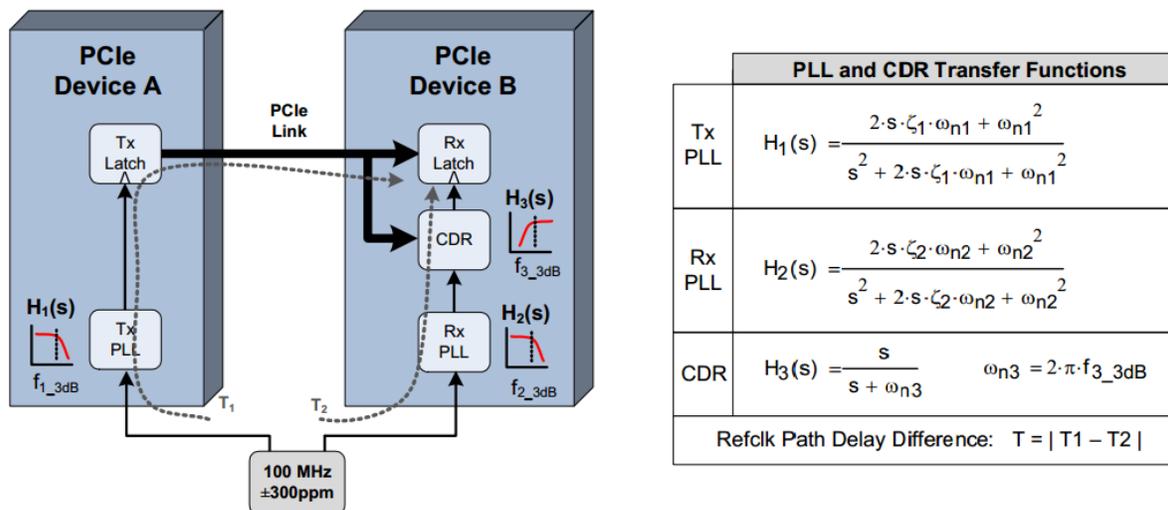


Figure 1 Example serial link illustrating the importance of jitter transfer functions [1]

Strictly speaking, PLLs are nonlinear filter systems; however, it is possible to model their behavior as linear transfer functions as shown in Figure 1. The theory behind these transfer functions is somewhat complex and the salient point in this paper is that parameters such as ω_n and ζ are critical to the operation of digital SerDes links at Gbps speeds. For example, having too much peaking (as affected by ζ) or having a large mismatch in ω_n between transmitters and receivers can have a catastrophic effect on link BER performance.

Measurement Concept: Sine Wave In, Sine Wave Out

Illustrated in Figure 2, the **SV1C** will be used in this paper to perform jitter transfer measurement. The **SV1C** is ideal for this purpose because it includes high precision calibrated jitter injection sources, and it contains parallel jitter measurement channels and post-processing engines. The integration of all of these functions in an instrument form factor that fits in the palm of one hand affords great flexibility in analyzing multiple transfer functions in complex links such as that in Figure 1. Specifically, and referring to Figure 3, the **SV1C** is used to automatically execute the following sequence of steps shown in the figure. First, calibrated sine wave jitter waveforms are generated as stimulus to the PLL under test or CDR under test. Then, the PLL response to the sinusoidal input is measured. This response is itself generally sinusoidal in nature as well, although its amplitude and phase will depend on the frequency-selective nature of the PLL under test. Finally, **Introspect ESP** automatically analyzes the output and input sine waves collectively in the frequency domain, performs the automated sweep across the target frequency range, and constructs the desired result.



Figure 2 SV1C Personalized SerDes Tester used for jitter transfer measurement

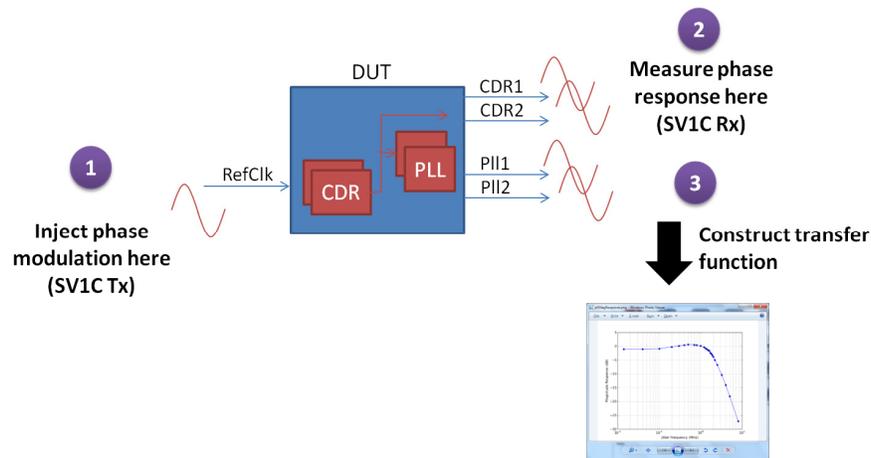


Figure 3 Jitter transfer functions based on sinusoidal phase modulation and measurement

The concept of Figure 3 is extremely simple, and it is enabled by the automation tools in **Introspect ESP** and by the availability of versatile calibrated jitter sources in the **SV1C**. Specifically, the jitter being generated from the **SV1C** is already self-calibrated. Thus, when it is used to measure the response of a PLL, the tool already knows what the PLL input jitter waveform looks like, which results in significant time savings: in the past, one had to measure the jitter injection source first using, say, an oscilloscope before applying this jitter to the PLL and measuring its output using the same oscilloscope.

Measurement Concept: Serial Stream or PLL?

In modern high-speed links, the PLL is often embedded deep inside a processing element or network component. This was already evident in Figure 1 where the Tx PLL is used as a clock source for a Tx Latch that is sampling payload data to be communicated over the link. From a jitter transfer measurement perspective, the implication is that one is often required to measure the effect of the PLL on data passing through the link and not the PLL clock signal itself. As shown in Figure 4(b), the concept of stimulus and capture in this case is very much similar to that which was described in Figure 3. The only difference is that the **SV1C Rx** channel now analyzes the sinusoidal jitter modulations on arbitrary data streams and not clock-like signals. Apart from this, the **SV1C Tx** channel is programmed the same way, generating a clock reference to the DUT and injecting calibrated jitter waves as required by the sequence of Figure 3.

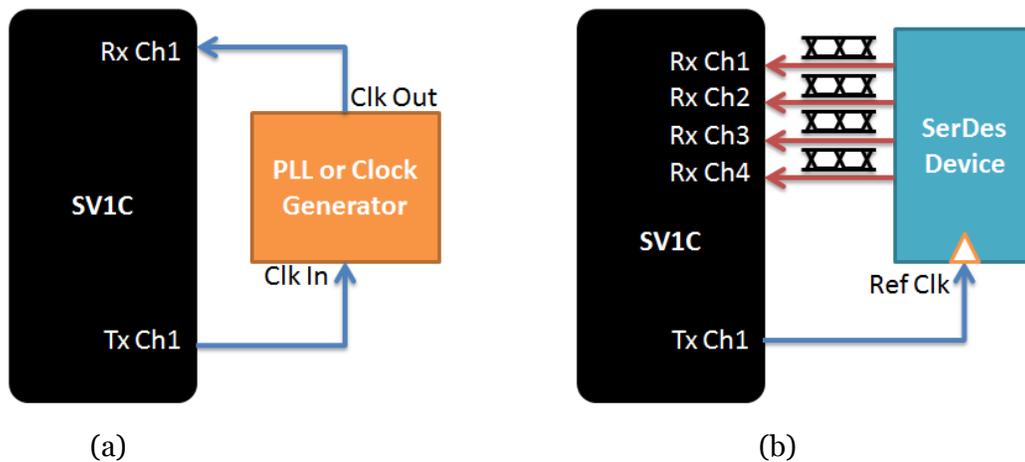


Figure 4 Illustration of the difference between measuring (a) a “clock” system, or (b) a complex SerDes device that has a reference clock input and internal PLL circuits. In (b), the measurement of output sine waves happens on data signals and not clock waveforms

The Entire Procedure

We now describe the **SV1C** Test Procedure that is required to obtain a jitter transfer function on a high-speed PLL or SerDes link. In Figure 5, a Test Procedure consisting of 12 lines of code is shown. The `globalClockConfig.setup()` initializes the test and synthesizes the proper time base for the entire measurement. Then, the `txChannelList1.setup()` command creates a clock

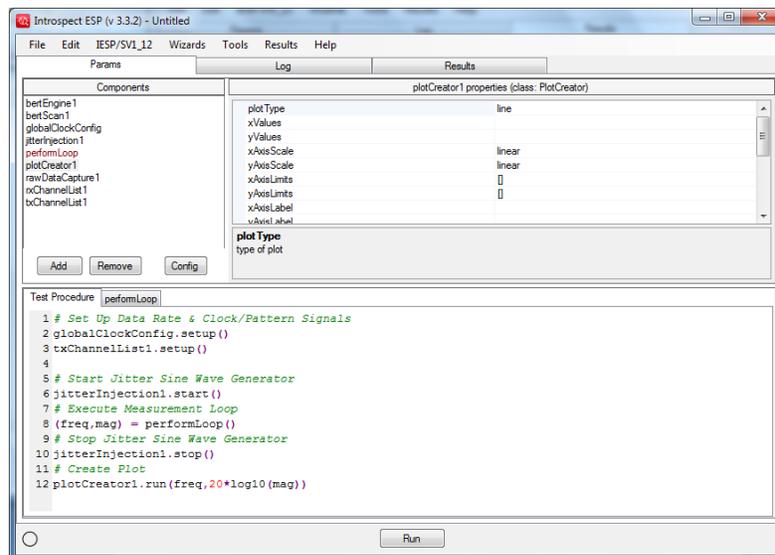


Figure 5 Introspect ESP Test Procedure for rapid PLL jitter transfer test

waveform that represents the direct stimulus (input clock or reference clock) to the PLL under test. Jitter injection is started at an initial condition that does not cause disruption to the PLL, and then the measurement loop is executed.

Note that the software components described above are applicable for testing a wide range of PLLs since the **SV1C** contains flexible frequency synthesis and data pattern handling capability. Similarly, if the DUT was a SerDes link with actual payload data, then the rxChannelList1 programming would have been adjusted accordingly to measure a digital pattern instead of a clock.

Experimental Results

The results of executing the Test Procedure of Figure 5 are described in this section. Figure 6 shows the entire transfer function for a single PLL that was measured. This graph was generated automatically after execution of the Test Procedure. As can be seen, a low pass function is observed with a 3dB frequency of about 9 MHz. We also see that there is about 1 dB of peaking around the frequency of 2 MHz.

It is important to note that each solid circle in the graph of Figure 6 is an explicit execution of the sinusoidal input/output sequence described in Figure 3. To illustrate this, we show bathtub plots in Figure 7 for both the input and output signals of the PLL at one iteration in the loop. The input signal has a very wide jitter lobe

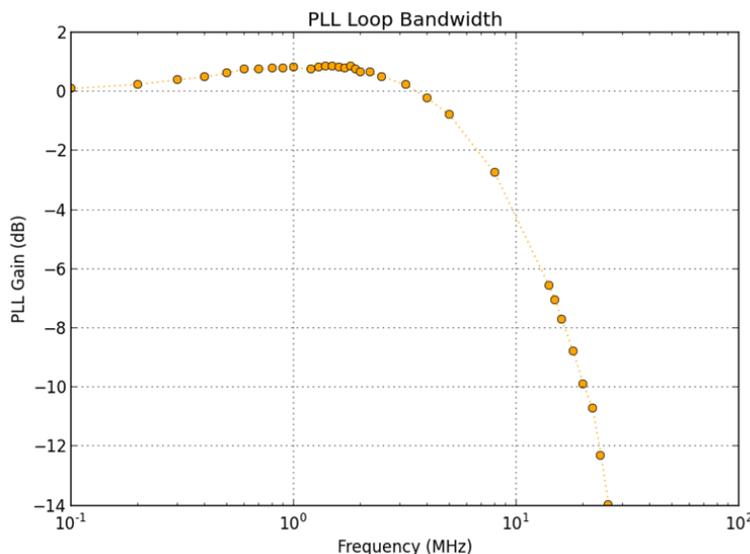


Figure 6 Automatically generated PLL transfer function as a result of the execution of Test Procedure

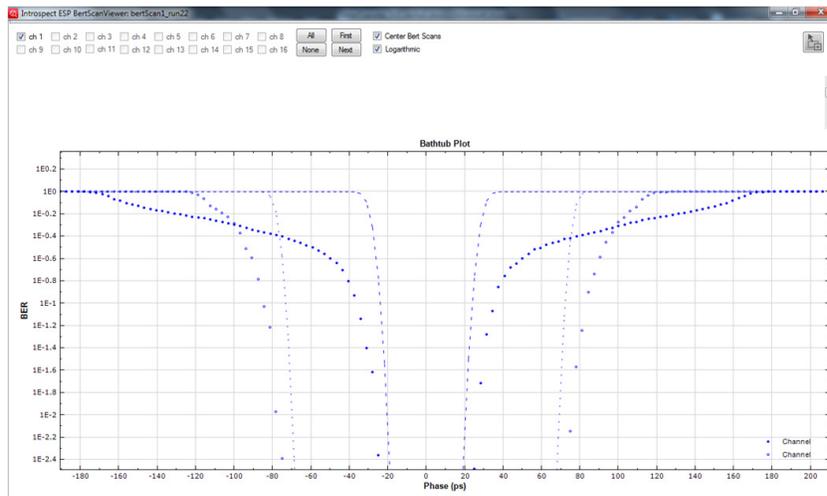


Figure 7 Bathtub plots representing input and output phase modulation: dark blue is input modulation, light blue is output modulation after being attenuated

that is typical of sinusoidal jitter; on the other hand, the output of the PLL has a much narrower lobe because the jitter is largely attenuated by the PLL at that particular frequency. The Test Procedure simply analyzed results such as these for all points on the graph of Figure 6.

Advanced Topics

With the basic transfer function collection process described, we can now proceed to performing much more elaborate characterization steps with the **SV1C** on other devices under test. In Figure 8, we show the result of testing another device across its VCO frequency range. The figure shows two transfer functions, one at the minimum VCO frequency and one at the maximum VCO frequency. Both bandwidth and peaking are altered slightly as is typical of ring oscillator PLLs. This figure was obtained by creating an outer loop to the Test Procedure of Figure 5 in which the `globalClockConfig.setup()` component was iterated on to generate stimulus signals at different frequency values.

In Figure 9, a CDR frequency response is illustrated. The transfer function is now a high-pass function as shown by the large attenuation at low frequencies and low attenuation at high frequencies. Also introduced in this figure is the concept of time-domain phase modulation analysis in which the **SV1C** is used to explicitly measure both the input and output time-domain sinusoidal waveforms. This offers the unique opportunity to

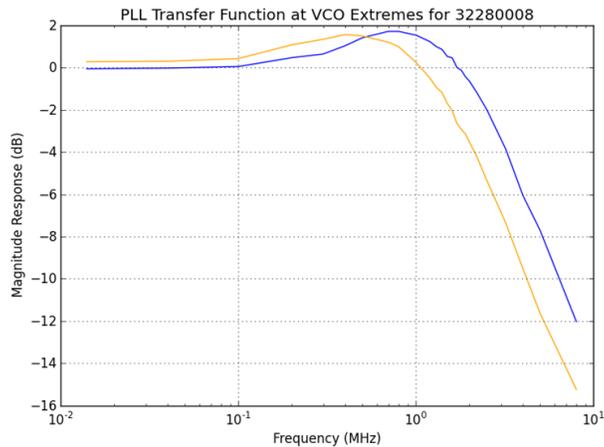


Figure 8 Automatic characterization of PLL across its entire operating range

understand and analyze nonlinear effects in circuits or to correlate physical measurements to time-domain SPICE simulations of the circuits. In the figure, we see that a reasonably linear input sinusoidal waveform to the CDR has not only been attenuated by the CDR filter function, but it has also been distorted. As mentioned earlier in this paper, distortion is inevitable in PLL circuits, and the figure offers an opportunity to scrutinize the distortion and correct it if necessary. Finally, Figure 10 shows a parallel measurement in which three traces are collected simultaneously.

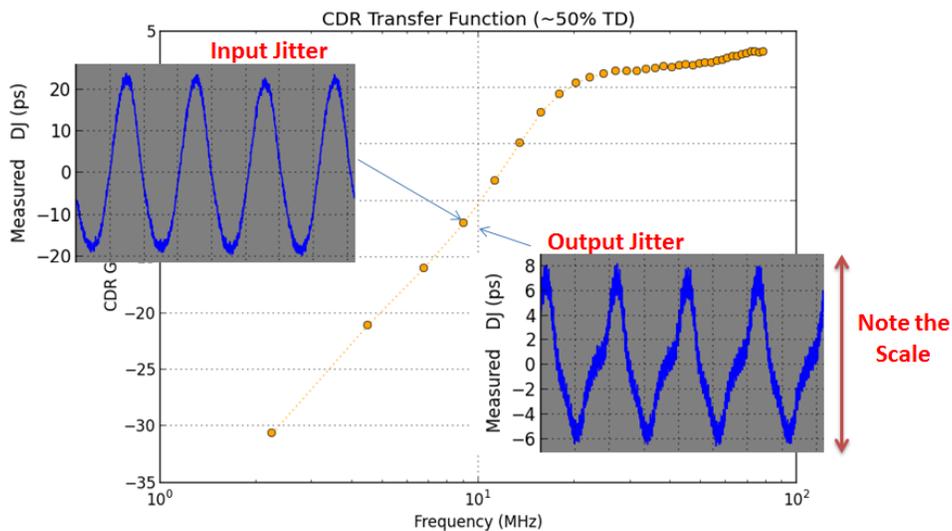


Figure 9 Time-domain response and linearity analysis of critical jitter components

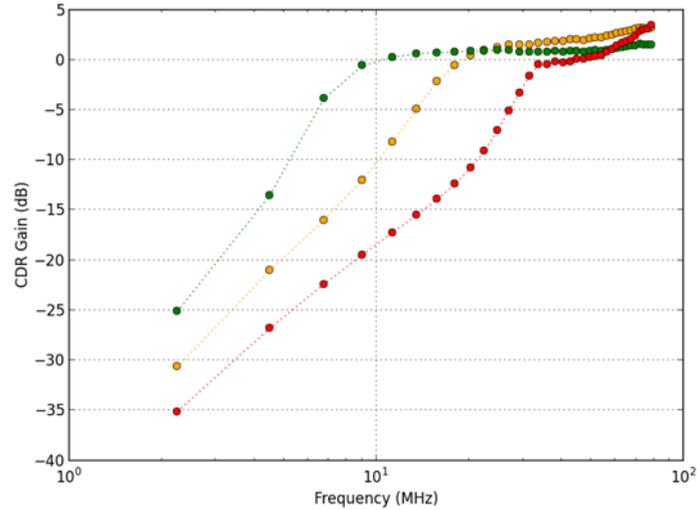


Figure 10 Parallel jitter transfer measurement

Conclusion

In this paper, we have used the **SV1C** to perform rapid and highly flexible jitter transfer testing on PLLs and CDR circuits. We described the importance of jitter transfer testing, the measurement concept deployed, and simple Test Procedures for data collection. We also showed advanced analysis topics including time-domain measurement and parallel measurement.

References

[1] Silicon Laboratories, AN562, www.silabs.com